08/771,708

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/771,708	12/20/96	HARARI	E

LM41/0331

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EXAMINER	
HUA, L	

ART UNIT	PAPER NUMBER
2785	6

DATE MAILED: 03/31/98

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☑ Responsive to communication(s) filed on December 20, 1996, February 13, 1998 and February 2, 1998.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☑ Claim(s) 1-99 is/are pending in the application.

Of the above, claim(s) 1-62 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☐ Claim(s) 63-70, 71, 72, 74-85, 87-93 and 95-99 is/are rejected.

☑ Claim(s) 73, 82, 83, 86 and 94 is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☑ See the attached Substitute of Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☑ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☑ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☑ Notice of Reference Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☑ Substitute of Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

– SEE OFFICE ACTION ON THE FOLLOWING PAGES –

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following elements must be shown or the feature(s) canceled from the claim(s):

a. the "reset circuit" recited in claim 82;

b. the "means for verifying the individual threshold level ranges of the plurality of memory cells after the cells have been programmed into the individual threshold level ranges beyond one of their breakpoints by a margin" recited in claim 86; and

c. the " register" recited in claim 94.

No new matter should be entered.

2. The abstract of the disclosure is objected to because its contents are not directed toward the subject matter which the applicant intended to claim. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities: the initialized correction at lines 11-12 of page 5 is confusing in that it is not clear whether hand written phrase is to be inserted or to replace the phrase in the parentheses. Appropriate correction is required.

4. Claims 73, 82, 83, 86 and 94 are objected to because of the following informalities. Appropriate correction is required.

a. <u>With regard to claim 73:</u>

The specification fails to specifies the feature of "simultaneously changing the threshold levels of cells within a selected two or more blocks to said given level range". To over come this rejection the applicant is requested to point out the specification section that describes such feature.

b. With regard to claim 83:

The phrase "the plurality of addressed cells are less that a number of cells within the individual blocks" appear to contain grammatical error and thus cannot be clearly understood. Correction is required.

c. With regard to claims 82, 86 and 94:

The elements recited in these claims are not shown in the drawings.

5. The obviousness-type double patenting rejection is a judicially established doctrine based upon public policy and is primarily intended to prevent prolongation of the patent term by prohibiting claims in a second patent not patentably distinct from claims in a first patent. In re Vogel, 164 USPQ 619 (CCPA 1970).

6. A timely filed terminal disclaimer in compliance with 37 C.F.R. § 1.321(b) would overcome an actual or provisional rejection on this ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 C.F.R. § 1.78(d).

7. Claims 63-70, 72, 74--85, 87-93 and 95-99 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims 27, 28, and 48-65 of U.S. Patent No. 5,172,338.

a. As per claim 63:

i. Claim 63 of the present application claims:

A method of operating an EEPROM system having memory cells that individually include(s) an electrically floating gate carrying a charge level that is alterable in response to appropriate voltage conditions being applied to the cell in order to set a variable threshold level thereof into a range that is determinable by reading the cell, said method comprising:

(1) applying said appropriate voltage conditions in parallel to a plurality of said memory cells, thereby to alter the charge levels on the floating gates of said plurality of memory cells,

(2) determining the threshold level ranges in which individual ones of said plurality of memory cells lie, and

(3) terminating said application of appropriate voltage conditions to individual ones of said plurality of memory cells upon their being determined to have reached desired threshold level ranges while continuing to apply said appropriate voltage conditions to others of said plurality of cells until all of the plurality of cells are determined to have reached their desired threshold level ranges.

ii. The steps of claim 63 of the present application are substantially claimed to be of the components of claim 27 of the Patent.

iii. It would have obvious to a person having ordinary skill in the art at the time the invention was made to recognize that the functional steps performed in combination are the step of the method of claim 63 of the present application.

iv. Thus, if claim 63 of the present application is allowed, this claim would extend patent coverage of the claim 27 of the patent.

v. Furthermore, there is no apparent reason why applicant was prevented from presenting the claim in the present application for examination during the prosecution of the application of patent.

b. As per claim 82:

i. Comparing claim 82 of the present application with claim 27 of the patent:

(1) the EEPROM system corresponds to IC chip of claim 27 of the patent;

(2) the array, [which is (I) of electrically alterable memory cells that individually include a field effect transistor having a floating gate and a threshold level that is variable in accordance with an amount of charge carried by the floating gate, and (ii) being divided into blocks of cells that are resettable together, cells within said blocks being addressable for application of programming voltage

conditions to individually charge/program them into one of more than two distinct threshold level ranges corresponding to more than one bit of input data per cell], corresponds to the patent's array of EEPROM cells;

(3) the programming circuit [that applies the programming voltage conditions to a plurality of addressed cells within a reset block to drive the effective threshold voltage of the addressed cells toward one of the more than two programmable threshold level ranges] corresponds to the patent's means for programming in parallel a stored chunk of data into the plurality of addressed cells;

(4) the reading circuit [that monitors in parallel the threshold level ranges of the plurality of addressed cells] corresponds to the patent's means for verifying; and

(5) the control circuit [that individually terminates application of the programming voltage conditions to any one of the plurality of addressed cells when the reading circuit verifies that said any one cell has reached the programmable threshold level range that corresponds to the input data being stored therein, while enabling further application of the programming voltage conditions to others of the plurality of addressed cells that have not yet been so

verified, until all of the plurality of addressed cells are verified] corresponds to the patent's improvement.

ii. The reset circuit [that applies simultaneously reset voltage conditions to the cells within individual blocks to drive the effective threshold levels of such cells to a reset state], which is recited in claim 82 of the present application, is not explicitly stated in claim 27 of the patent. This reset circuit, however is implied to be in the claim of the patent, which implication is denoted by the open-end word "comprising" used in the preambles of the claim of the Patent. [The applicant is hereby informed that the reset circuit is not shown in the drawings and the objection of such is indicated above].

iii. Thus, if claim 82 of the present application is allowed, this claim would extend patent coverage of the claim of patent 5,172,338.

iv. Furthermore, there is no apparent reason why applicant was prevented from presenting the claim in the present application for examination during the prosecution of the application of the patent.

c. As per claim 95:

i. Claim 95 of the present application claims:

a method of storing multiple bits of binary data in a chunk of non-volatile memory cells which individually have more than two programmable states,

comprising:

(1) applying electrical programming parameters in parallel to cells within said chunk,

(2) monitoring the states of individual cells within said chunk, and

(3) terminating

application of programming parameters to individual cells within said chunk

when they are monitored to have reached desired ones of said more than two programmable states corresponding to the multiply bits of data being stored,

while continuing

to apply said programming parameters to others of the cells within said chunk,

until all of the cells within said chunk are determined to have reached their programmable states corresponding to the multiple bits of data being stored.

ii. The steps of claim 95 of the present application are substantially performed by the components of claim 27 of the Patent.

iii. A person having ordinary skill in the art would have recognized that the combination of the steps of the components of claims 27 of the patent is a method for storing multiple bits of binary data in a chunk of non-volatile memory cells.

iv. Thus, if claim 95 of the present application is allowed, this claim would extend patent coverage of claim 27 of the patent.

v. Furthermore, there is no apparent reason why applicant was prevented from presenting the claim in the present application for examination during the prosecution of the application of the patent.

8. Claim 99 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 27 of U.S. Patent No. 5,172,338.

a. As per claim 99:

i. The various elements of the claims of the present application and the various combination thereof are substantially claimed the claim 27 of the Patent. Comparing claim 63 of the present application with Claim 27 of the patent:

(1) the EEPROM system correspond to patent's integrated circuit chip.

(2) the integrated circuit array of electrically alterable memory cells corresponds to the patent's array of EEPROM cells;

(3) the programming circuit corresponds to the patent's means for programming in parallel a stored chunk of data into the plurality of addressed cells;

(4) the reading circuit that verifies corresponds to the patent's means for verifying;

(5) the last two claimed elements [i.e., (a) means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and (b) the means for (I) further programming and verifying in parallel the plurality of addressed cells and (ii) inhibiting programming of correctly verified cells until all the

plurality of addressed cells are verified correctly] corresponds to the patent's improvement.

ii. The following features of claim 63 of the present application are not not explicitly recited in claim 27 of the patent:

(1) the EEPROM cells are individually programmable into more than two states, thereby individually storing more than one bit of binary data];

(2) the programming circuit's application of appropriate programming parameters in parallel to an addressed plurality of cells; and

(3) the reading circuit's verification

(a) is done in parallel and

(b) is to verify the state into which the addressed plurality of cells are programmed.

iii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize that:

(1) the EEPROM cells of claim 27 of the patent are individually programmable into more than two states (thereby individually storing more than one bit of binary data) ---- this is because the preamble of claim 27 of the patent states that each of the addressable EEPROM memory cells:

(a) has its own (I) a source, (ii) a drain, (iii) a control gate and (iv) an erase electrode receptive to specific voltage conditions for (1) reading, (2) programming and (3) erasing of data in the cell, and

(b) has its own a floating gate that is capable of retaining a specific charge level corresponding to a specific memory state of the cell, (such that a specific memory state is achieved by increment/decrement of the charge level with successive applications of programming/erasing voltage conditions);

(2) the programming circuit of claim 27 of the patent applies (in parallel) programming parameters to the plurality of addressed cells---- this is because the preamble of claim 27 of the patent states that each of the addressable EEPROM memory cells is (I) receptive to a specific voltage condition for programming, (ii) capable of retaining a specific charge level, corresponding to a specific memory state of the cell, and (iii) a specific memory state is achieved by incrementing the charge level with successive applications of programming voltage conditions; and

(3) the verification of the reading circuit of claim 27 of the patent is:

(a) done in parallel ---- this is because patent states that the means, which is in the improvement, is for allowing further parallel verification, which "further allowance" implies (as supported by the specification of the patent) that the initial/previous/latest verification done by the reading circuit is also done in parallel; and

(b) done to verify the state into which the addressed plurality of cells are programmed ---- this is because the statement, "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data" (in claim 27 of the patent) is understood (as is supported by the specification of the patent) to be for the purpose of verify the state into which the addressed plurality of cells are programmed.

iv. Thus, if claim 63 of the present application is allowed, this claim would extend patent coverage of the claim 27 of the patent.

v. Furthermore, there is no apparent reason why applicant was prevented from presenting the claim in the present application for examination during the prosecution of the application of the patent.

b. <u>As per claim 64</u>:

Claim 51 of the patent provides the same limitation to claim 27 of the patent as claim 64 of the present application to claim 63 of the present application. That limitation is that there are exactly two threshold level ranges.

c. As per claim 65:

Claim 50 of the patent limits a feature of claim 27 of the patent as claim 65 of the present application limits that of claim 63 of the application. That limitation is that there are more than two threshold level ranges.

d. As per claim 66:

Claim 53 of the patent limits a feature of claim 27 of the patent as claim 66 of the present application limits that of claim 63 of the application. That limitation is that the threshold level ranges are separated by exactly one breakpoint threshold level.

e. As per claim 68:

Claim 63 of the patent limits a feature of claim 27 of the patent as claim 68 of the present application limits that of claim 63 of the application. That limitation is that

the desired threshold level ranges include an erased threshold level range.

f. As per claim 70:

i. The statements, [i.e., "individual ones of the blocks include a specific number of memory cells" and "the plurality of memory cells to which the

appropriate voltage conditions are applied in parallel are less than the specific number" recited in claim 70], is [by definitions for the term "blocks"/"chunks" and for the phrase cells- to-which- the- appropriate-voltage-conditions-are-applied, which definitions are defined by both of the specification of the patent and the specification of the present application] are also true for those term and phrase of claim 27 of the patent.

ii. Additionally, the repeating [i.e., furthering] for another plurality of cells within the one block the applying, determining & terminating operations is clearly covered by claim 27 of the patent by understanding that the "further applying" is corresponding to the "repeating".

g. As per claim 72:

i. Claim 28 of the patent limits claim 27 of the patent as claim 72 of the present application limits that of claim 63. Claim 28 of the patent states that the system of claim 27 is on an IC chip.

ii. The skilled person would have realize that the steps performed by the system on an IC chip is carried out on the integrate circuit chip.

h. As per claim 74:

By definition, a single given threshold level range to which cells [that can be charged/discharged to at least two definite threshold level ranges] can be charged/discharged is within one of said at least two defined threshold

level ranges. This definition is true for both the single/specific state of the cells in the claims of the patent and the single/specific state of the cells in the claims of the present application.

i. As per claim 75:

By definitions of programming and erasing [in term of charging and discharging as in both the specification of the patent and the specification of the present application] EEPROM cells as that of claim 27 of the patent, it is understood that the cells of claim 27 of the patent reaches their desired ones of said threshold level ranges by applying appropriate voltage conditions to the plurality of memory cells correspond to a chunk of input data being programmed into the memory system.

j. As per claim 77:

i. Official notice is hereby taken that temporarily storing input data, which is to be stored into a memory destination, into a cache memory prior to storing them into the memory destination is a common practice in the art.

ii. It would have been obvious to one having ordinary skill in the art at the time the invention was made to store the chunk of input data into a cache memory prior to being programmed into memory cells within the EEPROM. This is because the caching provide efficiency in term of processing time for higher information transfer rate. Notice that in both of the claim of the present application and claim 27 of the patent: (a) the

system, having the input data in the cache, would not have to reobtain the input data from the source of the input data; and (b) the input data is needed again and again for the continuously repeated programming.

k. As per claim 78:

Claim 55 of the patent further limits a feature of claim 27 of the patent as claim 78 of the present application limits that of claim 63 of the present application. The limitation is that the voltage conditions, that are appropriately applied to said plurality of memory cells, are applied in successive applications of said voltage pulses that individually shift the threshold level of the cells to which the voltage pulses are applied less than one half of a difference between adjacent ones of the breakpoint levels.

l. As per claim 79:

The feature of programming memory cells to within a desired threshold levels by a margin is covered by claim 52 of the patent. The cells' marginal reaching to that desired threshold levels is the situation in which the application of the appropriate voltage conditions to individual ones of the plurality of memory cells is to be terminated.

m. As per claims 76, 80 and 81:

Both claims 49 and 56 of the patent limit a feature of claim 27 to comparison of memory output with expected reference for determining whether cells have been programmed to desired threshold levels.

n. As per claim 83:

The definition of phrase "the plurality of addressed cells" (in claim 27 of the patent) has a specific meaning as defined by the specification of the patent. The number of cells within the individual blocks is also specifically defined by the specification of the patent. Those two definitions should correspond with the same in the present application. Therefore, the statement "the plurality of addressed cells are less that a number of cells within the individual blocks" in claim 83 of the present application is, by definition, true for claim 27 of the patent.

o. As per claim 84:

The control circuit include's elements, [i.e., (I) a plurality of latches and (ii) means for setting individual ones of the latches in response to corresponding ones of said plurality of addressed cells being verified], are not explicitly stated in claim 27 of the Patent. However, these elements are implied to be in the claim 27 of the Patent, which implication is denoted by the open-end word "comprising" used at line 47 of the claim 27 of the Patent.

p. As per claims 67 and 85:

Claim 54 of the patent limits a feature of claim 27 of the patent as claim 67 of the present application limits that of claim 63 of the application. That limitation is that the threshold level ranges are separated by more than one breakpoint threshold level.

q. As per claim 87:

i. the programming circuit's causing of addressed cells to be programmed with successive applications of said programming voltage conditions have been addressed in the rejection of various claims above.

ii. the reading circuit's operation [to monitor the threshold level ranges of the plurality of addressed cells in between applications of said programming voltage conditions] is covered by the broad recitation of claim 27 [col. 26, lines 44-46] as that operation is specified in the specification of the patent to be of the reading circuit.

r. As per claim 88:

Claim 55 of the patent covers the feature of claim 88. That covered featured is that the programming circuit shifts the threshold levels of the individual addressed cells by less than one half of a difference between at least two breakpoint threshold levels.

s. As per claim 89:

Claim 57 of the patent covers the programming circuit's operation with programming voltage conditions that requires a plurality of said successive

applications of programming voltage conditions in order to change individual ones of the plurality of addressed cells from one of the threshold level ranges to another adjacent threshold level range.

t. As per claim 90:

The control circuit's comparator, [which (a) receives (I) the monitored threshold level range of the plurality of addressed cells, and (ii) the input data being programmed into the plurality of addressed cells and (b) for verifying when the individual ones of the plurality of cells reach the programmable threshold level that corresponds to the input data being stored therein], is covered by claim 49 of the patent and is corresponding to the means for comparing in that claim.

u. As per claim 91:

Claim 59 of the patent covers the features of claim 91 of the present application, [those features are: (1) the at least one reference cell is included in individual ones of the blocks of cells, (2) which additionally comprises means for programming said at least one reference cell to a reference level, and (3) said reading circuit includes means for reading the reference level of the reference cell of the block wherein the plurality of addressed cells exists to verify that any one cell has reached the desired threshold level range].

v. As per claim 92:

Claim 63 of the patent limits a feature of claim 27 of the patent as claim 92 of the present applicant to that claim 63 of the application. That limitation is that a reset circuit includes means operable after application of the reset voltage conditions to an addressed at least one block for adjusting to the reset state any cells of said at least one block that were over erased by the reset voltage condition application.

w. As per claim 93:

The reset circuit's two elements, [i.e., (1) the means for selecting one or more of the blocks for erase, and (2) the means, which is responsive to the selection means, for simultaneously applying the reset voltage condition to the memory cells within all of the selected blocks], are covered by claim 64 of the patent.

x. As per claims 69, 96 and 97:

The combination of claims 64 and 65 of the patent limits a feature of claim 27 of the patent as claim 96 and 97 of the present application limits that of claim 95 of the application. That limitation is that the cells within said chunk are all reset to one specific programmable state (i.e., a reset/erased state).

With regard to the phrase "prior to applying electrical programming parameters to the cells within said chunk," a skilled person in the art would have recognized that prior to writing a chunk of data into

a chunk of EEPROM cells the charged voltage levels in the cells should be discharged so as to protect the cells from being overcharged/destroyed due to the sum of the existing charge already in the cells and the additionally programmed charge.

y. As per claim 98:

It would have been obvious to a skilled person to make sure that the discharging is correctly done and thus operate the of claim 27 to:

(1) applying electrical programming/discharging parameters in parallel to at least the cells within said chunk,

(2) monitoring the states in which at least the cells within said chunk are individually programmed/discharged, and

(3) terminating application of programming/discharging parameters to individual ones of at least the cells within said chunk when they are monitored to have reached said one of the more than two programmable states while continuing to apply said programming/discharging parameters to others of the cells within said chunk until all of the cells within said chunk are determined to have reached the reset one of the more than two programmable states.

9. Claim 71 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims 27, 28, and 48-65 of U.S. Patent No. 5,172,338 as applied to claim 69 above and further in view of the claims of patent number 5,297,148.

As per claim 71:

a. The claims of patent number 5,297,148 teaches:

   i. individual ones of the blocks/sectors of cells contain a number of spare cells,

   ii. the spare cells within a particular block/block are substituted in place of any defective cells within said plurality of cells of said particular block.

b. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add the spare-cells-feature of the 5,297,148 patent in the blocks/sectors of the 5,172,338 patent. This is because:

   i. the 5,297,148 teaches such additional feature in the blocks/sectors of an EEPROM; and

   ii. the additional feature would provide reliability to the EEPROM memory system.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703)305-9724 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert W. Beausoliel, Jr., can be reached on (703) 305-9713. The fax phone number for this Group is (703) 305-9724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

LY V. HUA
PATENT EXAMINER
ART UNIT 2785

L. Hua
March 13, 1998